IN THE SPECIFICATION

Please amend paragraph [0046] as follows:

[0046] Figs. 14a and b is a diagram of bias circuits and delay lines according to the prior art.

Please amend paragraph [0071] as follows:

[0071] In [f]Figure 14a, a [two] prior art voltage control bias circuit[s] and VCDL[s] [are] is shown. In a [the first of these] circuit[s] **500**, delay lines consist of a positive bias line **554** and a negative bias line **552**. The positive bias line **554** is coupled to a current mirror consisting of transistors **512** & **514**. The negative bias line **552** is coupled to a current mirror consisting of a transistor **520.** Transistor **512** is coupled via a resistor **516** to a voltage to current converter **526** formed of a transistor **518** and resistor **522.** The circuit is biased by a lower voltage **524** coupled to resistor **522** and transistor **520** and a higher voltage coupled to the transistors **512** and **514.** The input voltage **550** is coupled to transistor **518**. The purpose of resistor **516** is to limit the maximum frequency of operation. Phase offset information is asserted as the charge pump voltage onto the input **550**.

Please amend paragraph [0072] as follows:

[0072] In Figure 14b [As] an alternative to circuit **500** is shown. A circuit **502** consists of a positive bias line **554** and a negative bias line **552**. The negative bias line **552** is coupled to a current mirror consisting of transistors **528** & **530**. The positive bias line **554** is coupled to a current mirror consisting of a transistor **536.** Transistor **528** is coupled via a resistor **532** to a voltage to current converter **540** formed of a transistor **534** and resistor **538.** The circuit is biased by a lower voltage **524** coupled to the transistors **528** and **530** and a higher voltage coupled to resistor **538** and transistor **536.** The input voltage **550** is

coupled to transistor **534**. The purpose of resistor **532** is to limit the maximum frequency of operation. Phase offset information is asserted as the charge pump voltage onto the input **550**. The difficulty with both the prior art bias circuits is a vulnerability to process mismatch distorting the response of the delay line. This contributes to jitter.